SINGLE-BOARD WAVELET VIDEO COMPRESSION/DECOMPRESSION UNIT

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Abstract: *The system described is based on the wavelet video compression/decompression method, implemented on a single board and tailored for a real-time work. Different bit-rates are supported in the full-duplex mode and in the range from 8-50 Mbit/s. Specific solution of the internal DMA transfer between the compressor/decompressor and the transmission FIFO buffers is described. Some considerations on the constant bit-rate implementation are given. An example for a live video transmission on an SDH loop is shown.*

Key words: *wavelet compression/decompression, video transmission, fix-rate transmission channels.*

1. INTRODUCTION

Wavelets are basis functions that separate data into different frequency components, in order to analyse each component with a selected resolution matched to its scale [1]. Unlike the Discrete Cosine Transform DCT that is by its definition non-local and therefore can not reproduce sharp discontinuities in a signal, wavelets approximate finite domains and are appropriate for analysing choppy signals [2].

While DCT compression schemes (e.g. MPEG-2) have to break each image into sub-blocks, a wavelet-based compression analyses the entire image eliminating block artefacts and offering graceful image degradation at higher compression ratios. The availability of full image sub-band data enables further image processing with little or no computational overhead. The advantages of wavelet-based compression have been recognised also in standardised JPEG2000 specifications.

Real-time compression techniques have to be symmetrical (the complexity of analysis has to be similar to the complexity of synthesis), the algorithms should take into account the human visual model. A constant bit-rate or constant quality has to be

achieved. All mentioned issues can be implemented by wavelet methods in a very efficient way [3]. The practical result based on wavelet technology is commercially available in a single-chip for compression and decompression of digital video signals in real-time from Analog Devices ADV601 [4].

In the rest of the paper a short presentation of the wavelet video compression/decompression board is presented. Some implementation details of DMA data transfer between the ADV601 and transmission FIFO buffer are emphasised. Next, a constant bit-rate compression method is described. An application example is given finally, using the presented video board within an SDH transmission system.

2. VIDEO BOARD FUNCTIONS

Some basic functional blocks of the video board and signal interfaces between these blocks are shown in Figure 1. Two independent channels of opposite directions are supported by the digital signal processor ADSP2185. It runs on 62.5 ns instruction cycle time with up to seven wait states for memory access. In the compression path, a standard PAL television signal is converted into 4:2:2 digital component video data compatible with the CCIR656 10-bit extended standard using video decoder ADV7185. The digital video stream is fed into the video codec ADV601 that operates in the compression mode. The actual transmission of the compressed stream between the ADV601 and the transmission FIFO buffer is implemented by a custom designed DMA controller. Control registers of the DMA controller and both video codecs are accessed by the DSP through 8-bit address bus and 16-bit data bus. Video codecs and the DMA controller operate on 27 MHz internal clock. In the decompression path the described process is reversed.

Optimal utilisation of the available communication media, particularly in applications with higher bit-rates, requires a DMA controlled data transfer because the compressed video stream is issued in data bursts with a non uniform speed. The DSP processor is trying to adapt the compression ratio dynamically in order to achieve the constant bit-rate, however, a transmission FIFO is still needed to fully utilise a fix-rate G.703 data channel capacity. With the adaptive compression method the resulting bit-rate of the compressed video stream can approach, in longer time periods, to the requested fixed rate or equivalently to the average size of a target frame. The DMA controller, FIFO buffers and all remaining logic with a loop-back feature are implemented within two FPGAs. The DSP processor controls video encoder and decoder chips using I^2C compatible bus. Video RAM is added for testing purposes and for possible extensions in the future use. Overall operations of the compression module are monitored by an external system through the RS232 compatible interface.

The digital signal processor is used for configuration of board components, handling some of the exceptions, that are caused by FIFO overflows or underflows and by both codecs, for communication with an external system through the RS232 compatible interface, and for maintaining constant long-term bit rate in the compression path. The last task requires an on-line computation of compression ratios using video field statistics and current bit-rate. The compression ratios or bin-width values must be

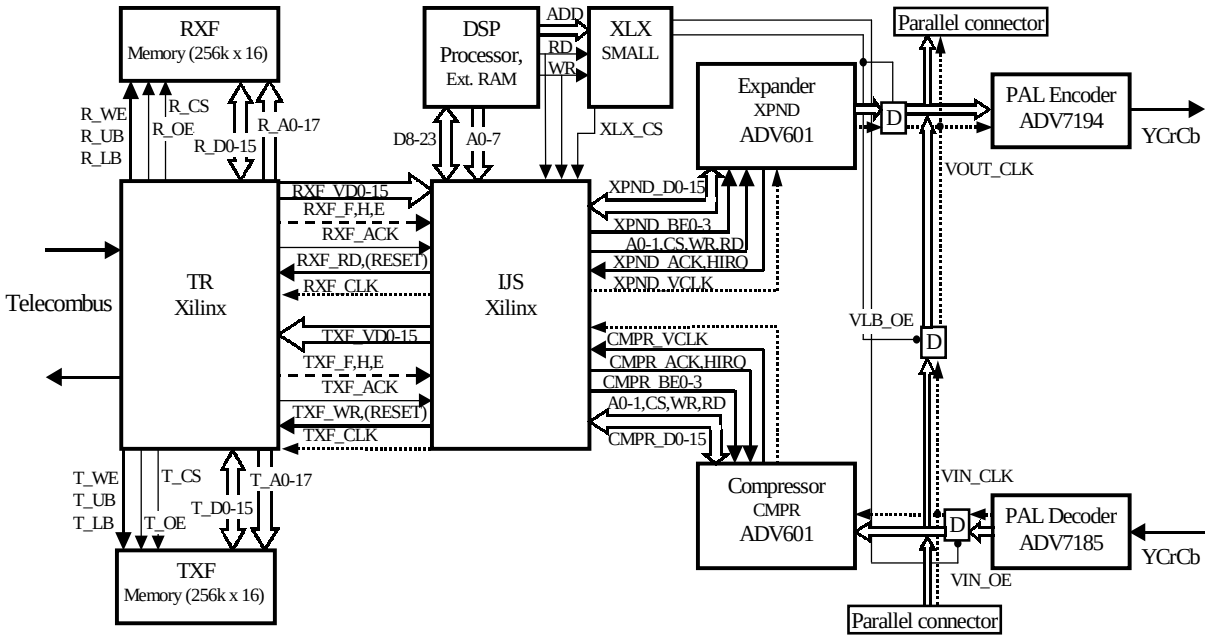

Fig. 1. The block diagram of wavelet based video compression/decompression board.

written into the ADV601 compressor registers on a field by field basis. Most of these tasks interfere with DMA operations.

The data transfer is a simple but a time-consuming task. It would be a waste of resources to use the DSP instead of DMA controller to assist the the data transfer. By higher data rates, the DSP could not perform this task adequately. The DMA logic waits for available data, performs data transfer and waits again for a confirmation. Because the buses to both codecs are shared between the DSP and FIFO, a DSP read or write requests form/into a codec register may interrupt the video stream transmission. The DMA logic of the compression path is given in Figure 2. by a final state automata. It is composed of four loops: waiting, compressor read, compressor write and FIFO write. The longest loop lasts six states in the worst case. The current synchronous implementation allows a burst transmission with tree states, resulting in a speed of up to 144 Mbit/s. The DMA logic of the decompression path is implemented in a similar way. Further improvements would be possible, by shortening the longest loop, but they are not needed because the internal buffering in ADV601 still allows the specified minimal compression ratios.

3. CONSTANT BIT-RATE COMPRESSION

A video signal with small number of details results in a low wavelet compressed bit-rate, however, a lot of sharp edges and contrast details will usually produce much higher bit-rates. If a simple scene changes to a complex one, bit-rate will change substantially which is not appropriate for a fixed rate transmission channels. The wavelet module

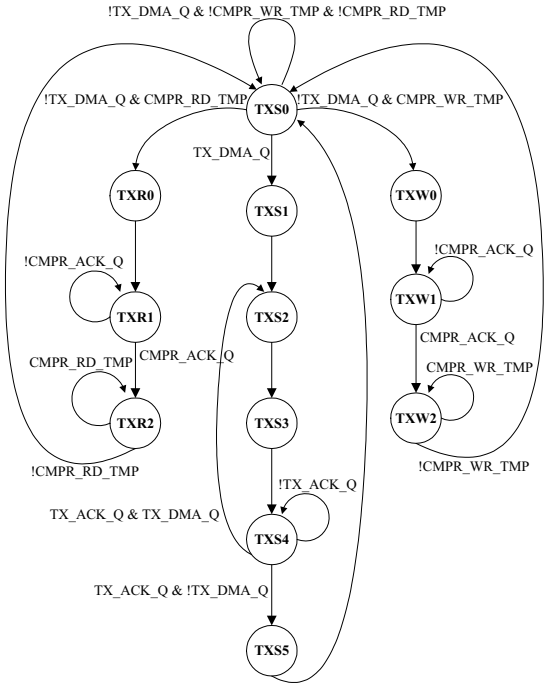

Fig. 2. The states of DMA controller for the compression data path.

solves this problem by a DSP processor that controls the compression ratio and adapts it on-line to achieve a desired constant bit-rate.

The wavelet compression is done by quantization in frequency space that bases on the discarding of less important bits in different data blocks belonging to different frequency bands. The DSP processor must change the quantization level in real-time by observing previous results of compression and the properties of a new image. Basically, the size of the previous compressed field has to be subtracted from the size of a target field and on the basis of this difference the bin-width values have to be calculated for the actual field [5]. On every field, sum of these differences is updated. If the DSP is capable of keeping this sum near zero, then in long term, a constant bit-rate can be achieved. The transitions between different compression levels are implemented by a servo-loop routine. It has to keep the mentioned sum of differences in a specified interval. The quantization level is chosen on the basis of this sum. If it becomes greater than zero, more data could be transferred, while, if it becomes smaller, there is too much data, so the compression ratio should increase. The method described would suffice if a very fast DMA data transfer is available. But because we have limited speed of DMA, the bin-width calculator must be implemented in a more reliable way.

In an interrupt routine, the DSP processor reads ADV601 registers, to obtain the size of the last compressed field and the statistical characteristics of the field already filtered but not compressed yet. It computes the differences between statistical characteristics of the current field and the previous field. If the scene changed, the difference will be usually greater than a given limit. As a consequence, the compressed video will

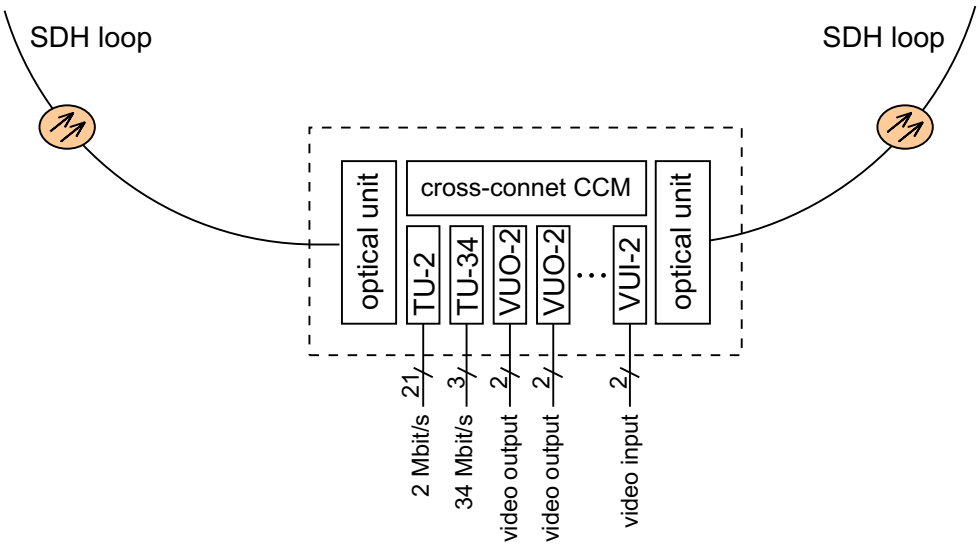

Fig. 3. An application example of the video board in an SDH loop.

drastically change and special measures have to be taken for the bin-width calculation. According to the characteristics of the servo loop, higher compression will be used for the current and some of the following fields. The fact is that the processor does not know if the first field form the new scene will really give more data as the previous field, but this is expected with an average 50If the compression was to high and the compressed data are smaller than expected, no big harm was done, servo loop will adapt the compression dynamically within some next fields and restore the requested average broadcast quality. On the other hand, if the servo loop would not be in action, the compressed field data could become too big to be correctly conducted by the DMA unit. So, on any substantial scene changes the compression level will always increase, presumably higher than necessary, just to stay on the safe side.

4. APPLICATION EXAMPLE

An target application example of the wavelet compression/decompression module is shown in Figure 3. Two independent channels that can be configured separately, allow a full duplex video transmission. Communication multiplexer combines video, audio, synchronisation and control data into an SDH virtual container VC3 with an approximate raw bit-rate of 48 Mb/s.

5. CONCLUSION

We described some possibilities for a real-time digital video transmission over fixed rate communication channels. A custom designed FIFO buffer and DMA controller are needed for the transmission of a professional video quality by an optimal utilisation of the available communication media. New applications are possible by adopting the DSP software. High compression ratios allow to enter the applications in the

surveillance area, on the other hand, low compression ratios enable the transmission of a professional video.

REFERENCES

[1] M. Vetterli, J. Kovacevic: *Wavelets and Sub-band Coding*, Prentice Hall, 1995.

[2] K. Jack: *Video Demystified, A Handbook for the Digital Engineer*, Second Edition, HighText Interactive, Inc., San Diego, 1996

[3] R. Trobec, R. Novak, I. Ozimek, G. Kandus: Compressed Image Transmission on Fix-Rate Digital Channels, *Proceeding VIPromCom-2001*, Zadar 2001, 203-207.

[4] A. Zatsman et al.: Industry's First Integrated Wavelet Video Codec Sets New Standards for Cost, Image Quality and Flexibility, *Analog Dialogue* 30-2, 1996.

[5] D.Starr: ADV601 Binwidth Calculation in 21xx DSP, *Analog Devices Application note*, Januar 1997.